SUMMARY

Temperature rise due to Joule heating of on-chip interconnects can severely affect performance and reliability of next generation microprocessors. Thermal predictions become difficult due to number of features on the order of a billion and the impact of electron size effects on electrical and thermal transport. It is thus necessary to develop efficient numerical approaches and accurate metal and dielectric thermal characterization techniques. In this research, analytical, numerical, and experimental techniques were developed to enable accurate and efficient predictions of temperature rise in an on-chip interconnect stack.

A finite element based compact thermal modeling methodology was developed to obtain temperature rise with lesser number of elements and acceptable accuracy (5 - 10 %). In this technique, the temperature drop across the interconnect cross-section was ignored. This approach was applied to two-dimensional uniformly spaced interconnects, three-dimensional interconnects terminated with vias, and a real world structure consisting of a long serpentine chain of about 500 interconnects and vias. In all the cases, the compact model performed better than standard finite elements. In some cases, the performance was improved by an order of magnitude. The compact model predictions agreed closely with experimentally measured temperature rise of the serpentine chain.

A numerical solution was developed for electron transport through complex interconnect structures based on the Boltzmann Transport Equation (BTE). This deterministic technique, based on the path integral solution of BTE within the relaxation time approximation, free electron model, and linear response, was applied to a constriction in a finite size thin metallic film. Effective conductance dropped over the bulk value even with specular surface scattering for different constriction sizes and aspect ratios. An extension of the constriction results for a short metallic bridge was discussed. These simulations can provide effective resistances between two locations, and can then be used in a macroscale framework.

An Atomic Force Microscope (AFM) was used to develop a new technique to measure thermal conductivity of thin metallic films in the size effect regime. This technique uses Scanning Joule Expansion Microscopy (SJEM) to measure temperature expansion amplitude on the surface of a constriction in a thin film. It does not require complex microfabrication to obtain free-standing structures, and thus preserves the original metal interface and scattering characteristics. Using extensive thermal conduction modeling in the frequency space, thermal conductivity values for two structures were extracted from SJEM measurements. The thermal conductivities of 43 nm and 131 nm gold films were found to be 82 W/mK and 162 W/mK respectively at the smallest frequency investigated. These measurements were close to Wiedemann-Franz Law predictions and are significantly smaller than the bulk value of 318 W/mK due to electron size effects. The technique can potentially be applied to interconnects in the sub-100 nm regime.

A semi-analytical solution for the 3ω method was derived to account for thermal conduction within the metallic heater. Existing uniform heat flux approximation between the metal heater and substrate was replaced by a more realistic uniform heat generation condition within the metal heater. Although this correction does not affect thermal conductivity measurements in the original 3ω method, it is shown that significant errors can result when it is applied for anisotropy measurements. For small thermal conductivity films, the error in the anisotropy ratio can be as high as 50 %.